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Memorandum

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Subject: **Updated Description and Recommendations for the ERC32 Chip-set Synchronous and Asynchronous Fault Handling and Trap Generation**

CONTENTS

WARNING

The TSC693E User Manual from ATMEL (Rev. D, 10 Apr. 97) has precedence over the present document.

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List of changes in the issue 1 revision 3

The text of the bullet 3 and the text of the bullet 5 of the paragraph 5 have been updated to match exactly the figure 1. The end statement of the paragraph 5, and the recommendations in the paragraph 6 are left unchanged.

1 Scope of the Document

The purpose of this document is to clarify the description of the ERC32 Chip-set handling of the synchronous and the asynchronous faults and the trap generation and to make recommendations in order to guarantee a reliable handling of the ERC32 Chip-set synchronous and asynchronous faults.

2 Reference Documents

REF1: TSC691E Integer Unit User's Manual
ATMEL
Rev. I
23 Sep. 98

REF2: TSC692E Floating Point Unit User's Manual
TEMIC
Rev. H
02 Dec. 96

REF3: TSC693E Memory Controller User's Manual
TEMIC
Rev. D
10 Apr. 97

3 Background

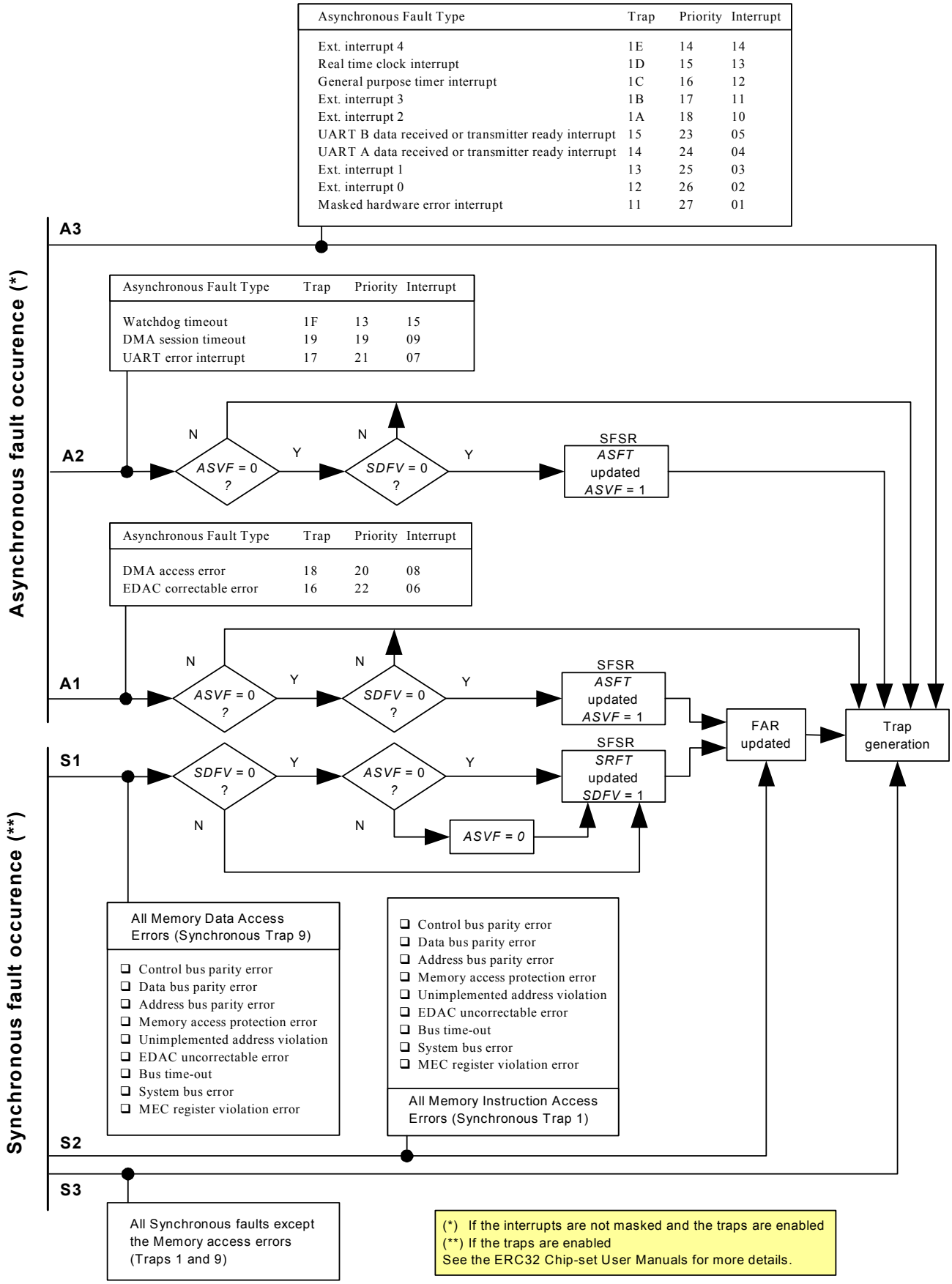
As the result of a detailed review by ESA and ATMEL of the description of the ERC32 handling of the synchronous and the asynchronous faults and the corresponding trap generation it has been found necessary to clarify the description provided in the ERC32 Chip-set (TSC691, TSC692, TSC693) User's Manuals that are referenced above.

4 Description of the ERC32 Chip-set Handling of the Faults and the Trap Generation

The following Figure 1 presents a synthetic description of the handling of the synchronous and the asynchronous faults and the corresponding trap generation by the ERC32 Chip-set for all the cases.

Figure 1

ERC32 Chip-set Diagram for all Synchronous and Asynchronous Faults and Trap Generation



5 Analysis of the ERC32 Chip-set Handling of the Faults and the Trap Generation

From the previous Figure 1 the following remarks and conclusions can be derived:

***Note**: In the following text the class fault codes make reference to the classes that are identified on the left side of the previous Figure 1.*

- All synchronous and asynchronous faults will generate a trap *but not all of them will update* the System Fault Status Register (SFSR) and the Failing Address Register (FAR) of the ERC32 Chip-set
- The faults of the class A3 and the class S3 *never update* the SFSR and the FAR
- The faults of the class A2 (traps 17, 19, 1F) *will only update* the SFSR, *but*:
  - If there was a previous class A1 or A2 faults the SFSR *will not be updated*
  - If there was no previous class A1 or A2 faults but there was a previous S1 class faults (trap 9) the SFSR *will not be updated*
- The faults of the class S2 (Trap 1) *will always update* the FAR *only*
- The faults of the class A1 (traps 16 and 18) *will update both* the SFSR and the FAR *but*:
  - If there was a previous class A1 or A2 faults the SFSR and the FAR *will not be updated*
  - If there was no previous class A1 or A2 faults but there was a previous S1 class faults (trap 9) the SFSR and the FAR *will not be updated*
- The faults of the class S1 (data access, Trap 9) *will always update both* the SFSR and the FAR independently of the previous class of traps.

Consequently for the A1 and the A2 cases it can be seen that the update of the SFSR and the FAR can be blocked either by a previous class A1 or A2 faults, or a by previous S1 class faults that will have set the *ASFV* or the *SDFV* bits to *one* in the SFSR.

6 Recommendations

To guarantee the update of the SFSR and the FAR in all possible fault sequences it is necessary to clear the relevant *ASFV* and the *SDFV* bits of the SFSR. Since the individual clearing of the *ASFV* and the *SDFV* bits of the SFSR is not possible it is necessary to reset the SFSR by writing any value to it. The reset value of the SFSR is 0x00000078 that corresponds to all the fields being cleared to the *zero* value except for the *SRFT* field that is set to all *one's* (reset value for the synchronous fault type).

Consequently, in order to guarantee the update of the SFSR and the FAR in all possible fault sequences, it is recommended to reset the SFSR on the exit of the following trap handlers:

9, 16, 17, 18, 19, and 1F.